

REMARKS

In the Office Action, the Examiner noted that Claims 1-20 are pending in the application and that Claims 1-20 are rejected. By this response, Claims 1, 8, 15, 17, and 19 are amended. In view of the above amendments and the following discussion, the Applicant submits that none of the Claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The Examiner objected to Claims 1, 8, 15, 17, and 19 as containing informalities. More specifically, the Examiner stated that the terms “timing attributes” and “timing parameters” need to be clarified to be more concise. The Examiner stated that the phrase “may be” should be replaced with concise claim language.

First, Claims 1, 8, 15, 17, and 19 have been amended to remove the phrase “may be”. Notably, in Claim 1, the phrase “may be placed” has been removed in favor of “is placeable.” In Claims 8, 15, 17, and 19, the phrase “may be applied” has been removed in favor of “is applicable.”

Second, the Examiner did not cite any law, rule, or regulation in objecting to the terms “timing attributes” and “timing parameters,” but rather stated that such terms are not “concise.” The Applicant contends that such terms are suitably concise and fully comply with the patent laws, regulations, and rules, including 35 U.S.C. §112. In particular, such terms are described in the specification in a manner that enables one skilled in the art to practice the invention. (See, e.g., Applicant’s specification, ¶¶0032 and 0038-0039). Moreover, the terms “timing parameters” and “timing attributes”, when interpreted in light of the specification by one skilled in the art, reasonably define the invention. Accordingly, Applicants respectfully request that the objection to Claims 1, 8, 15, 17, and 19 be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected Claims 1-5 as being anticipated by Srinivasan (United States patent application publication 2004/0196081, published October 7, 2004). In particular, the Examiner stated that Srinivasan teaches the elements of Applicants' Claim 1. (Office Action, pp. 2-3). The rejection is respectfully traversed.

Srinivasan teaches a hierarchical block for an integrated circuit having a clock cluster buffer for each cluster of sequential registers. In a given cluster, clock net connections can be made between clock pins of the registers and the clock cluster buffer. (Srinivasan, Abstract). Srinivasan discloses that clock skew and phase delay at each pin is substantially similar to the clock skew and phase delay at each other pin. (Srinivasan, p. 3, ¶0036).

Srinivasan does not teach each and every element of Applicant's Claim 1. Namely, Srinivasan does not teach or suggest "determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the circuit design is placeable." (Applicant's Claim 1). Srinivasan does not teach or suggest determining multiple sets of timing attributes for multiple locations of the circuit design within the integrated circuit. Rather, Srinivasan discloses a circuit structure that is configured to balance local clock skew, minimize clock phase delay, and realize maximum clock skew constraints. (Srinivasan, p. 5, ¶0075). There is no teaching or suggestion in Srinivasan that timing attributes for the circuit structure are determined for multiple placements of the circuit structure within the integrated circuit.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Srinivasan does not teach or suggest determining multiple sets of timing attributes for multiple placements of a circuit design within an integrated circuit, Srinivasan does not teach each and every element of Applicant's Claim 1. Claims 2-5 depend, either directly or indirectly, from Claim 1 and recite additional features therefor. Since Srinivasan does not anticipate Applicants' invention as recited in Claim 1, dependent Claims 2-5 are also not anticipated and are allowable.

Therefore, Applicants contend that Claims 1-5 are not anticipated by Srinivasan and, as such, fully satisfy the requirements of 35 U.S.C. §102.

III. Rejection Of Claims Under 35 U.S.C. §103

The Examiner rejected Claims 6-20 as being unpatentable over Srinivasan in view of Applicant's admitted prior art (APA). The rejection is respectively traversed.

More specifically, the Examiner conceded that Srinivasan does not disclose a template having a predefined routing topology. (Office Action, p. 5). The Examiner alleged, however, that since a template having routing topology would facilitate the routing process, it would have been obvious to use such a template in Srinivasan. (Office Action, p. 5). The Applicant respectfully disagrees.

First, Claims 6-7 depend from Claim 1 and recite additional features therefor. The combination of Srinivasan and APA does not teach, suggest, or otherwise render obvious Applicant's invention recited in Claim 1. As discussed above, Srinivasan does not teach or suggest determining multiple sets of timing attributes for multiple placements of a circuit design within an integrated circuit, as recited in Applicant's Claim 1. The APA generally describes FPGAs and timing analysis based on costs of physical resources. The APA is devoid of any teaching or suggestion of determining sets of timing attributes for placements of a circuit design. Since neither Srinivasan nor the APA teach or suggest Applicant's Claim 1, no conceivable combination of Srinivasan and the APA renders obvious Applicant's Claim 1. Accordingly, the Applicant contends that Claims 6-7, which depend from Claim 1, are patentable over the combination of Srinivasan and the APA and, as such, fully satisfy the requirements of 35 U.S.C. §103.

Second, the combination of Srinivasan and the APA does not teach, suggest, or otherwise render obvious Applicant's invention recited in Claim 8. Namely, the combination does not teach or suggest: (1) "determining sets of timing parameters for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the template is applicable;" and (2) "placing and routing the circuit design within the integrated circuit based on the template. The failure of the combination to teach or suggest item (1) has been

discussed above. With respect to item (2), Srinivasan teaches a circuit structure and does not teach or suggest a placement and routing process for a PLD. The APA generally describes placement and routing, and does not teach or suggest placement and routing using a template. Thus, no conceivable combination of Srinivasan and the APA renders obvious Applicant's Claim 1.

Claims 15, 17, and 19 each recite features similar to those recited in Claim 8 emphasized above. For the same reasons set forth above, the combination of Srinivasan and the APA does not render obvious Applicant's Claims 15, 17, and 19. Finally, Claims 9-14, 16, 18, and 20 depend, either directly or indirectly, from Claims 8, 15, 17, and 19 and recite additional features therefor. Since the combination of Srinivasan and the APA does not render obvious Applicants' invention as recited in Claims 8, 15, 17, and 19, dependent Claims 9-14, 16, 18, and 20 are also nonobvious and are allowable. Therefore, Applicants contend that Claims 8-20 are patentable over the combination of Srinivasan and the APA and, as such, fully satisfy the requirements of 35 U.S.C. §103.


CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 2, 2005.

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Signature